

Microwave Performance of Low-Power Ion-Implanted 0.25-Micron Gate GaAs MESFET for Low-Cost MMIC's Applications

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Abstract—Low-power microwave performance of an enhancement mode (*E*-mode) ion implanted GaAs MESFET is reported. The $0.25\text{-}\mu\text{m} \times 100\text{-}\mu\text{m}$ *E*-MESFET has a threshold voltage of $V_{th} = 0.0$ V. At 1.0 mW operation of power with a bias condition of $V_{ds} = 0.5$ V and $I_{ds} = 2$ mA, a noise figure of 0.85 dB with an associated gain of 15 dB was measured at 4 GHz. These results demonstrate the GaAs *E*-MESFET is an excellent choice for low power personal communication applications.

I. INTRODUCTION

PORTABLE personal communication systems require the continuous improvement of low unit cost, light weight, and long battery lifetime. These improvements can be realized by the development of ultra low power, low noise, and high gain microwave MMIC receiver microelectronics. Typical personal communication system demands will be for devices exhibiting a noise figure less than 1 dB with 10 dB of gain at 2 GHz, while drawing a low power of 0.5 mW to 2 mW. Depletion mode ion implanted GaAs MESFET's have shown extrinsic current gain cutoff frequencies above 100 GHz, minimum noise figure less than 1 dB, and associated gain better than 13 dB at 18 GHz [1], [2]. However, the power consumption for these devices is relatively high in the 10 mW to 100 mW range.

In 1989, a single-stage amplifier employing an enhancement mode MESFET dissipating about 10 mW, achieved a gain of 10 dB with a return loss of 14 dB at 0.9 GHz [3]. The direct ion implanted GaAs *E*-mode MESFET is a proven technology; and the best device choice for low power MMIC's because of its inherent manufacturability. Also the MESFET is much cheaper to produce than HEMT's as no epitaxial layer is required. This technology will result in highly reproducible low power and low cost MMIC's for use in personal communications. In this letter, we report on the microwave

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characterization of an enhancement mode GaAs MESFET operating at low power levels (0.75 to 5 mW).

II. DEVICE FABRICATION AND DC CHARACTERISTICS

The substrates used in this work were LEC-grown 3-inch semi-insulating GaAs (100) wafers. The n-type channel region for the MESFET's were formed by Si^{29} direct ion-implantation with 80 KeV and 30 KeV, to a dose of $6.5 \times 10^{12} \text{ cm}^{-2}$ and $2 \times 10^{13} \text{ cm}^{-2}$ respectively. A buried *p*-layer with Be ions beneath the n-type layer was implanted as well. Wafers were subsequently annealed at 850° C in a $\text{H}_2\text{-AsH}_3$ atmosphere without cap. The ohmic and the gate electrodes were formed by AuGe-Ni-Au and Ti-Pt-Au, respectively. The $0.25\text{-}\mu\text{m}$ "T" gates were defined by *e*-beam direct write by a Cambridge EBMF 10.5 on a three-layer PMMA process at 30 kV and 1 nA. The resist layer used was 10% PMMA/9% (PMMA-MAA)/10% PMMA. A single step development in 1:1 MIBK:IPA was carefully monitored with development test patterns. This process typically exhibits yields in excess of 95%. Other process steps, such as mesa, ohmic, and pad metal, were defined using a shallow UV contact aligner.

The device geometry is a two fingered gate with each finger having dimensions $0.25 \text{ }\mu\text{m} \times 50 \text{ }\mu\text{m}$ (for $100 \text{ }\mu\text{m}$ total gate width FET's). The drain current of the *E*-mode MESFET versus gate voltage for the fixed $V_{ds} = 1.5$ V is shown in Fig. 1. The breakdown voltage for the device was $V_{ds} = 6.0$ V. At $V_{gs} = 0.6$ V and $V_{ds} = 1.5$ V, the device achieves peak transconductance of 280 mS/mm at $I_{ds} = 9\text{mA} = 90\text{mA/mm}$ as shown in Fig. 1. The typical threshold voltage was found to be $V_{th} = 0.0$ V. When biased at $V_{ds} = 0.5$ V, $I_{ds} = 2$ mA the low power *E*-mode MESFET exhibited a transconductance of $g_m = 100$ mS/mm and an output drain conductance of $g_o = 8.75$ mS/mm. The ratio of g_m/g_o was 11 for 1.0 mW power operation.

III. MICROWAVE AND NOISE PERFORMANCE

A Hewlett Packard 8510 Network Analyzer System was used to measure the *s*-parameters of the device in a common source configuration. The device was tested on-wafer with

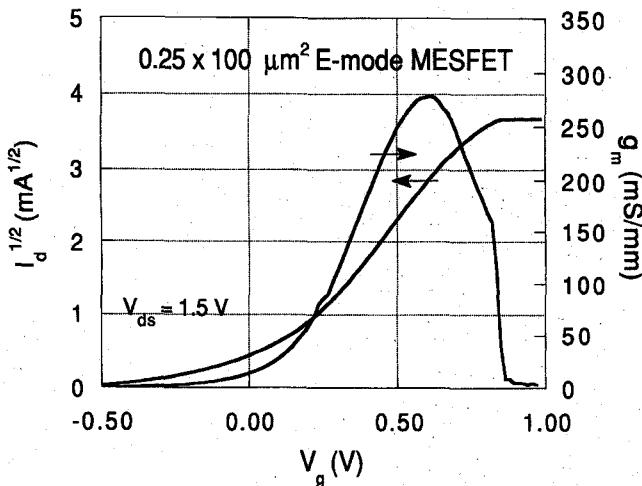


Fig. 1. Current and transconductance characteristics of a typical 0.25×100 micron gate GaAs *E*-mode MESFET.

Cascade Microtech probes. The small signal current gain H_{21} was calculated from the measured *s*-parameters. The $|H_{21}|$ was extrapolated to the unity gain frequency using a -6 dB per octave roll-off line in order to find the current gain cutoff frequency F_t of the device. The F_t and F_{\max} of the *E*-mode MESFET in low power operation (0.5 to 6 mW) are shown in Fig. 2. In this measurement, we fix $V_{ds} = 0.5$ V, 1.0 V, and 1.5 V, while varying V_{gs} (equivalent to varying I_{ds}) to change the power level from 0.5 to 6 mW. The device exhibited a peak F_t of 42 GHz biased at $I_{ds} = 4$ mA, and reached a maximum of 47 GHz at $I_{ds} = 9$ mA and $V_{ds} = 1.5$ V. The intrinsic F_t can be estimated as 62 GHz for the measured $F_t = 47$ GHz by subtracting parasitic pad capacitance [4]. The *E*-mode MESFET had a peak F_{\max} of 75 GHz. While drawing 1.0 mW of power, the device displayed a peak F_t of 25 GHz at $V_{ds} = 0.5$ V and $I_{ds} = 2$ mA. At this same bias, it achieved an F_{\max} of 50 GHz. The F_t of the device at a given power level increases with decreasing V_{ds} . For example, at $V_{ds} = 0.5$ V and $I_{ds} = 2$ mA the $F_t = 25$ GHz which was higher than the $F_t = 18$ GHz measured at a bias of $V_{ds} = 1.5$ V and $I_{ds} = 0.33$ mA.

The noise figure for the device was measured using a Cascade Microtech on-wafer noise parameter measurement system. The minimum noise figure and associated gain versus power at fixed $V_{ds} = 0.5$ V, 1.0 V, and 1.5 V for low power operation at 4 GHz is shown in Fig. 3. The error in the noise figure measurement was approximately 0.2 dB. For low power operation, the device worked best with a low voltage, high current bias. The device operating at 0.75 mW measured at 4 GHz achieved a noise figure of 0.8 dB, with a associated gain of 13 dB with $V_{ds} = 0.5$ V and $I_{ds} = 1.5$ mA. For the same power level, but with $V_{ds} = 1.0$ V, the noise figure increases to 1.7 dB with a associated gain of 10 dB. This observation agrees well with the increase in F_t with increase in drain current for a fixed drain voltage as shown in Fig. 2. The higher F_t values at low drain voltage predict better noise performance at this bias, since a higher F_t implies a lower noise figure according to the physical noise model developed by Statz *et al.* [5].

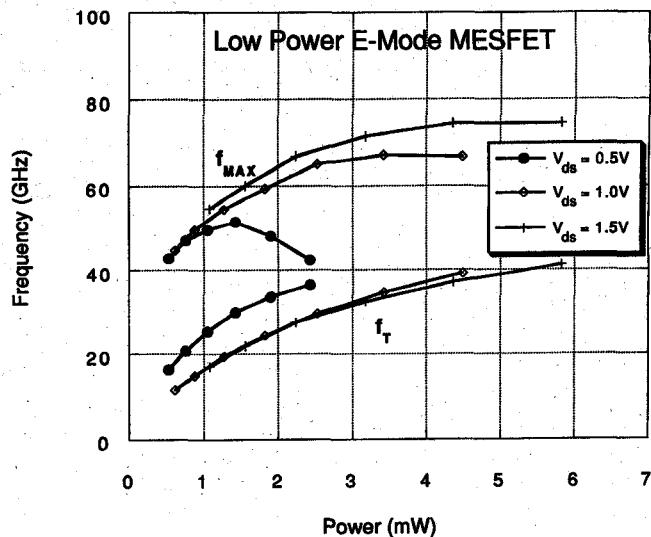


Fig. 2. Current gain cutoff frequency and maximum frequency of oscillation of a typical GaAs *E*-MESFET as a function of power operation.

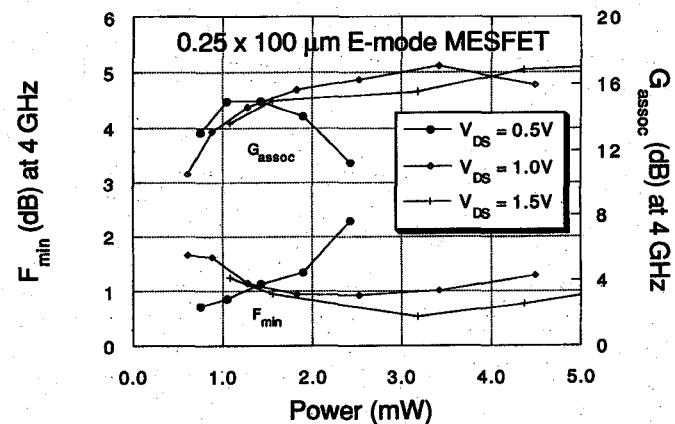


Fig. 3. Minimum noise figure and associated gain of atypical GaAs *E*-MESFET as a function of power operating at 4 GHz.

For the devices operating under $V_{ds} = 1.0$ and 1.5 V, the noise figure remains very close to 1 dB over the range between 1.5 to 4.0 mW, the corresponding associated gain increases from 15 dB at 1.5 mW to 17 dB at 3 mW operation. We observed the minimum noise figure to occur around 2 mA for several values of V_{ds} . Below 2 mA, the noise figure increased above 1 dB and the associated gain decreased. This is mainly due to an increase in source resistance and decrease in F_t at very low I_{ds} . The noise figure also increases for I_{ds} less than 2 mA for various V_{ds} bias. This effect is due to a fast increase in transconductance than the square root dependence of gate capacitance.

IV. CONCLUSION

The direct ion-implanted enhancement mode MESFET investigated in this work was demonstrated to be an excellent device choice for use in personal communications systems, as it clearly exhibited both high gain and low noise figure while operating at very low power levels.

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REFERENCES

- [1] M. Feng, J. Laskar, J. Kruse, and R. Neidhard, "Ultra low-noise performance of 0.15-micron gate GaAs MESFET's made by direct ion implantation for low-cost MMIC's applications," *IEEE Microwave Guided Wave Lett.*, vol. 2, no. 5, pp. 194-195, May 1992.
- [2] M. Feng and J. Laskar, "On the speed and noise performance of direct ion-implanted GaAs MESFET's," *IEEE Trans. Electron Device*, vol. 40, no. 1, pp. 9-17, Jan. 1993.
- [3] V. Nair, "Low current enhancement mode MMIC's for portable communication applications," *GaAs IC Symp.*, 1989, pp. 67-70.
- [4] M. Feng, C. L. Lau, and V. Eu, "An experimental determination of electron drift velocity in $0.5\mu\text{m}$ gate-length ion implanted GaAs MESFET's," *IEEE Electron Device Lett.*, vol. 12, pp. 40-41, 1991.
- [5] H. Statz, H. A. Haus, and R. A. Pucel, "Noise characteristics of gallium arsenide field-effect transistors," *IEEE Trans. Electron Devices*, vol. ED-21, pp. 549-562, Sept. 1974.
